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CIRCUIT SIMULATIONS OF A 1 MV LTD FOR RADIOGRAPHY

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Abstract

A 1 MV Linear Transformer Driver (LTD), capable of driving a radiographic diode load, has been built and tested. A circuit model of this accelerator has been developed using the BERTHA circuit simulation code. Simulations are compared to data from power-flow experiments utilizing a large area electron-beam diode load. Results show that the simulation model performs well in modeling the baseline operation of the accelerator. In addition, the circuit model has been used to predict several possible fault modes. Simulations of switch prefires, main capacitor failure, vacuum insulator flashover, and core saturation have been used to estimate the probability of inducing further failures and the impact on the load voltage and current.

I. INTRODUCTION

A seven cavity, 1 MV LTD was built to validate this accelerator technology as a possible driver for radiographic diode loads [1] [2]. Previous LTD designs produced pulses with risetimes in excess of 100 ns [3]. The 1 MV LTD was designed to produce greater than 100 kA critically damped current with a pulse width of approximately 45 ns measured at 80% peak voltage.

A photograph of one of the seven cavities from the 1 MV LTD is shown in Figure 1. The outer cover is removed to show the layout of the critical circuit components, which are arranged in groups referred to as bricks. Each brick consists of two 20 nF capacitors, charged to $\pm$100 kV, with a switch between them. The capacitance value was chosen to provide a short pulse with a fast risetme. Each cavity of the LTD contains 10 parallel bricks. The number of bricks was determined by the current requirement. Seven cavities are connected in series so the voltages add to approximately 1 MV. The pulse width was further reduced by adding five peaking capacitors to each cavity resulting in a pulse width of about 45 ns full width at 80% peak voltage. The peaking capacitors also increased the peak output voltage of each cavity. Due to failures, the system has been tested without peaking capacitors. The 1 MV LTD will be tested with redesigned peaking capacitors in the next few months.

Figure 1. Photograph of the inside of a single cavity of the 1 MV LTD.

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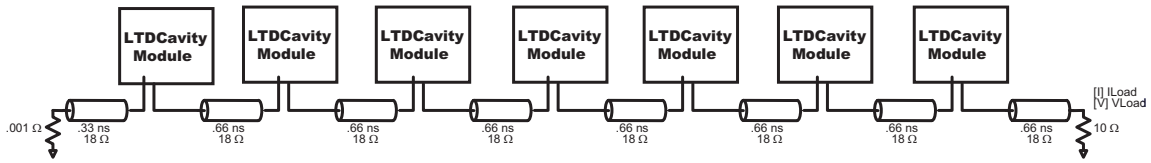

Figure 2. Diagram of the main BERTHA circuit file used to simulate the LTD. Each "LTD Cavity Module" block links to a circuit description of a single LTD cavity.

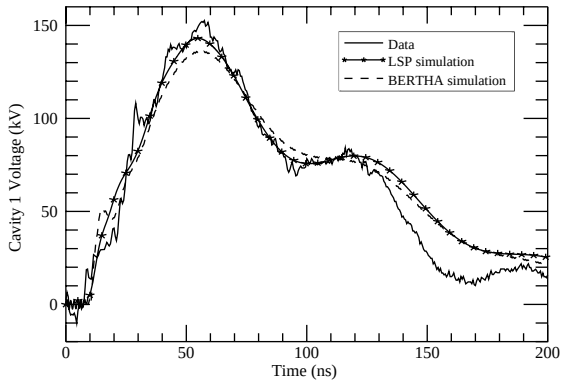

Figure 3. Comparison of simulations of the 1 MV LTD to Cavity 1 voltage measurements from experiments at HCEI.

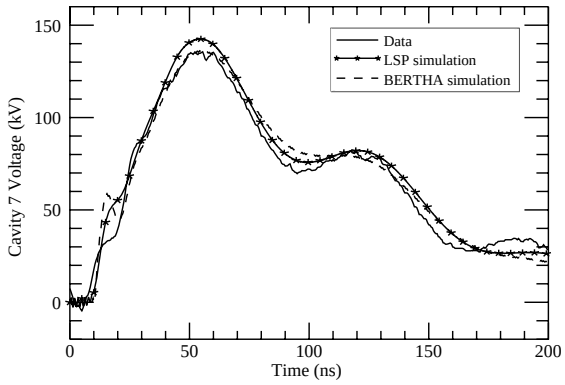

Figure 4. Comparison of simulations of the 1 MV LTD to Cavity 7 voltage data.

Voltage of the seven critically damped cavities is added along the central vacuum coax as parallel primaries coupled to a common secondary in a transformer. High permittivity steel cores within each cavity isolate the common grounds for the duration of the drive pulse. Voltage dividers are used to measure the output voltage at each of the seven cavities, while B-dot, V-dot and Rogowski coil probes mounted in two locations on the inner stalk and outer spool monitor the load conditions.

II. CIRCUIT SIMULATIONS

The BERTHA transmission line circuit code [4] was utilized to simulate the performance of the LTD. The BERTHA code incorporates the use of circuit modules, which function as circuit elements and link to a separate circuit file. This allows the user to create a complex model of a circuit element and use many instances of that module, passing distinct parameters to each of the separate modules. Each of the seven cavities was modeled individually as a single brick element, Figure 2, where the circuit component values were equal to the parallel combination of 10 bricks. This method of modeling all of the bricks in a cavity using the parallel combination of component values is much less complex than a model which represents each component individually and produced good results when compared to data, Figure 3. Where necessary for simulating individual brick performance and fault modes, the cavity model was expanded to simulate each individual brick. The expanded circuit model requires longer simulation time, and provides the same accuracy as the simplified model.

A simulation of the full seven cavity LTD including peaking capacitors is compared to experiments done at the High Current Electronics Institute (HCEI) in Tomsk, Russia with a large area diode load. Results of these tests with a 1.5 cm AK gap and a charge voltage of $\pm$ 90 kV are shown in Figures 3 and 4. These tests were done before transporting the LTD to Sandia National Laboratories (SNL). The BERTHA circuit very accurately predicts the output voltage of each cavity. The BERTHA cavity module was also used as the input to a LSP particle-in-cell [5] simulation of the coaxial vacuum section and large area diode load. The cavity voltages predicted by the LSP simulation also compare very well to experimental data. Both the BERTHA and LSP simulations accurately predict the voltage risetime, peak voltage, and the shape of the voltage decay.

After the initial testing of the LTD at HCEI, the seven cavities were shipped to SNL and reassembled. A 1.2 Ω load resistor was provided to allow each individual cavity to be tested to verify proper operation. During initial testing at SNL, a vacuum insulator and several peaking capacitors were damaged. Replacement parts were unavailable, so peaking capacitors were removed from all cavities and testing resumed with six series cavities. Approximately 100 shots have been fired with this six cavity configuration utilizing a large area diode load. Data from one of these experiments with a charge voltage of $\pm$ 95 kV and a AK gap of 2.5 cm is shown in Figures 5 and 6. The load voltage is approximated as the

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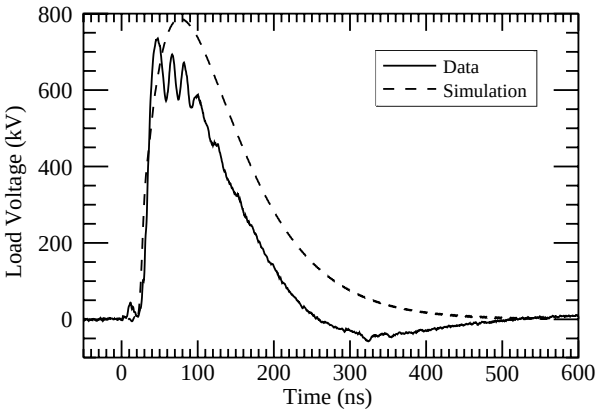

Figure 5. Comparison of a BERTHA simulation to the sum of cavity voltage measurements from experiments with six series LTD cavities.

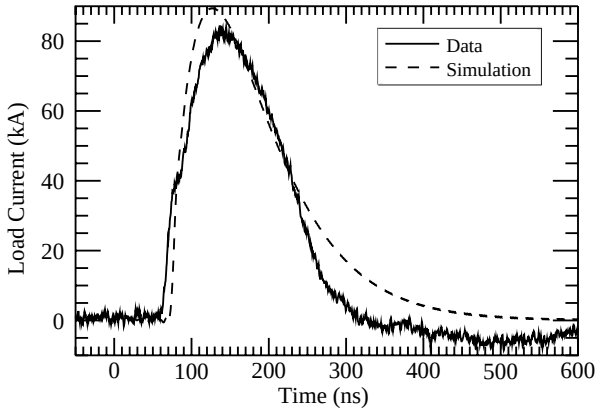

Figure 6. Comparison of a BERTHA simulation to Rogowski coil current measurements for a six cavity LTD shot at SNL.

sum of the resistive voltage divider measurements in each of the six cavities. The load current, plotted in Figure 6 is measured utilizing the Rogowski coil probe placed in the outer spool of the coaxial vacuum line approximately 73.5 cm from the diode. We have not yet determined why the BERTHA simulations do not match these preliminary results as well as they do the experiments done at HCEI with seven cavities.

III. FAULT MODE SIMULATIONS

Several possible failure modes of an LTD circuit have been identified. These include switch prefires, peaking capacitor failure, main capacitor failure, vacuum insulator flashover, and magnetic core saturation. Each of these failures has been simulated to determine the adverse effects on other parts of the circuit and on the load pulse. Some of these failures would require maintenance before the next shot to prevent damage to circuit components.

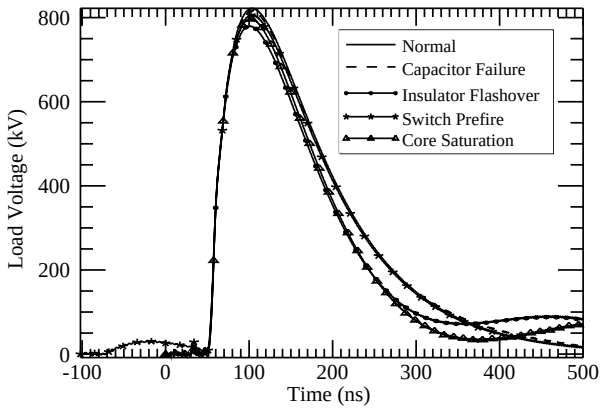

Figure 7. Comparison of simulated load voltages for various LTD fault modes. The peak load voltage is decreased by no more than 6% for any of the simulated faults.

However, in the simulated cases of a single cavity fault, the load voltage is not significantly effected, see Figure 7. The use of additional series cavities would further reduce the effect of a single failure on the load pulse.

Each of the fault modes was simulated for the current circuit configuration of six series cavities with no peaking capacitors. The BERTHA model of the LTD cavity was expanded to simulate each individual switch in all six cavities. Circuit models were also added to the cavity module to simulate insulator flashover, capacitor failure, and core saturation.

A. Main Capacitor Failure

A main capacitor failure was modeled by placing a wire in parallel with a single capacitor in one brick. The other capacitor in that brick used the normal capacitor model and it was assumed that the capacitor failure would not effect the switch operation. The simulation was performed to determine if a single capacitor failure would trigger additional capacitor failures or other problems in the circuit. Simulations indicate that a single shorted capacitor would cause the current through the other capacitor in the same brick to increase by about 50% and the current in other bricks in the same cavity to increase by about 10%. The increased current is well below the rated current for the capacitors. The voltage across the other capacitor in the brick with the shorted capacitor would reach a peak reversal of about 60%, which would decrease the capacitor life by about 22 shots for each reversal [6]. The capacitors are rated for 90% survival at 12,000 shots with 20% voltage reversal with typical LTD pulse shapes. The failure of a single capacitor would decrease the peak load voltage by less than 1%.

B. Insulator Flashover

Simulations of vacuum insulator flashover were performed by placing a switch with series inductance in parallel with the output of a single cavity. The simulation

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results in Figure 7 and described below are for an insulator flashover timed to occur at about 90% of the peak output voltage pulse. A surface flashover arc inductance of 30 nH was used, based on an estimate of 15 nH/cm and a 2 cm arc length. The simulation was used to determine if an insulator flashover would damage components within the cavity or increase the probability of insulator flashover in additional cavities. The insulator flashover produced a small peak in the voltage of the other five cavities, about 3% over the normal peak voltage, which would increase the probability of flashover from 6×10^{-6} for a normal pulse to about 8×10^{-6} using equation (1) [7]. Equation (1) estimates the probability of vacuum flashover, $f(t)$, based on the peak electric field stress (E), the effective pulse width (t_{eff}), the insulator circumference (C), a constant (β), and k defined as in equation (2) for an insulator thickness, d. The insulator flashover would also cause the main capacitor voltage for all capacitors in the cavity to reach a peak reversal of about 60%, resulting in the same lifetime decrease as reported above for a main capacitor failure. The insulator flashover reduces the energy that the cavity transfers to the load, consequently reducing the peak load voltage by about 6% and the pulse width by almost 4%.

$$f(t) = 1 - \exp\left(-\frac{E_p^{\beta} t_{\text{eff}} C}{k^{\beta}}\right) \tag{1}$$

$$k \equiv \frac{224 \exp\left(0.24/d\right)}{\left(\ln 2\right)^{1/\beta}} \tag{2}$$

C. Switch Prefire

The expanded cavity model described above allows the timing of each switch to be individually adjusted. Prefire of a single switch is simulated by setting the timing of one switch to time $t = 0$ and the remaining switches to fire at some later time. Simulation of several different timings showed that main capacitor voltage reversal, in the brick that prefires, is the most significant fault, and that this is maximized for a prefire delay of 127 ns. The capacitor voltage reversal of about 85% decreases the capacitor life by about 41 shots for each fault [6]. A single switch prefire results in an increased load voltage pre-pulse and a decrease of about 2% in the peak load voltage.

D. Core Saturation

Each cavity contains 8 iron transformer cores which are designed so that under normal operating conditions the cores will not saturate. If the cores are damaged, or not properly reset between pulses, the cores could saturate resulting in a low inductance discharge loop through the grounded cavity wall. A core saturation was simulated as a switch with series inductance in parallel with the cavity output. A simulated core saturation at 90% of the peak output voltage results in a cavity voltage reversal of about 85 kV, which exceeds the predicted flashover potential for a bipolar pulse, equation (3) [8]. The bipolar pulse flashover strength is determined using the pulse duration, t (μs), the insulator area, A (cm^2), and the insulator thickness, d (cm). The remaining five cavities are not significantly effected and would not have an increased probability of failure. The simulated core saturation would decrease the peak load voltage by about 3% and decrease the pulse width by about 4%.

$$E_{\text{bipolar}} = \frac{33}{t^{1/2} A^{1/10} d^{0.3}} \quad (kV/cm) \tag{3}$$

IV. SUMMARY

A circuit model of a 1 MV LTD has been developed using the BERTHA circuit code. The model has been compared to LTD tests performed at HCEI with very good agreement. Testing of the 1 MV LTD has begun at Sandia National Laboratories. Results of experiments with six series LTD cavities without peaking capacitors have been compared to simulations and efforts are underway to understand the discrepancies. The BERTHA model has been used to analyze possible fault modes that could occur during operation of the LTD. The simulated faults result in a decrease of less than 6% in the peak load voltage and no more than 4% in the pulse width. The effect of a single fault on the load voltage pulse would be further decreased with additional series cavities. While some of the simulated faults would increase the probability of component failure within the same cavity, none of the faults significantly increase the probability of faults in other cavities in the system.

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